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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/783,695	02/20/2004	Leonard Forbes	1303.019US2	1785

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SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. BOX 2938
MINNEAPOLIS, MN 55402-0938

EXAMINER	
SMITH, BRADLEY	

ART UNIT	PAPER NUMBER
2891	

DATE MAILED: 07/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/783,695	FORBES, LEONARD	
	Examiner	Art Unit	
	Bradley K. Smith	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-39* is/are pending in the application.

4a) Of the above claim(s) *35-39* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date ~~2/20/04~~, 11/22/04, 3/28/05 7/30/04
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *search notes*.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of claims 1-35 in the reply filed on 3/28/05 is acknowledged.

Information Disclosure Statement

1. The listing of references in the specification is not a proper information disclosure statement. 37 CFR 1.98(b) requires a list of all patents, publications, or other information submitted for consideration by the Office, and MPEP § 609 A(1) states, "the list may not be incorporated into the specification but must be submitted in a separate paper." Therefore, unless the references have been cited by the examiner on form PTO-892, they have not been considered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-35 are rejected under 35 U.S.C. 102(e) as being anticipated by Eldridge et al. (US 2005/0023603). With respect to claims 1, and 22, Eldridge et al. disclose a source region and a drain region separated by a channel region in a

substrate; a storage capacitor coupled to one of the source and drain regions (the examiner is taking official notice that this is well known in the art) ; a floating gate opposing the channel region; a gate oxide separating the floating gate from the channel region, the gate oxide having a first tunneling barrier height; a control gate opposing the floating gate; and a metal oxide insulator separating the control gate from the floating gate, the metal oxide insulator having a second tunneling barrier height, the second tunneling barrier height being less than the first tunneling barrier height, wherein the memory is adapted to operate the memory cell in a volatile memory mode and in a non-volatile memory mode. With regards to claim 2, Eldridge et al. disclose the floating gate includes a polysilicon floating gate having a metal layer separating the polysilicon floating gate and the metal oxide insulator, the metal layer in contact with the metal oxide insulator (see figure 2). With regards to claim 3, Eldridge et al. disclose wherein the control gate includes a polysilicon control gate having a metal layer separating the polysilicon control gate and the metal oxide insulator, the metal layer in contact with the metal oxide insulator (see figure 2) With regards to claim 4 Eldridge et al. disclose wherein the gate oxide includes silicon dioxide having a tunnel barrier height of about 3.2 eV (inherent) . With regards to claims 5-10 and 28-35, Eldridge et al. disclose the metal oxides (see abstract). With regards to claim 11, Eldridge et al. disclose an n+ channel layer (see figure 2). With regards to claim 12, Eldridge et al. disclose a source region and a drain region separated by a channel region in a substrate, a storage capacitor coupled to the drain region (well known to those of ordinary skill), a floating gate opposing the channel region, a gate oxide separating the floating gate from the

channel region, the gate oxide having a first tunneling barrier height; a control gate opposing the floating gate; a metal oxide insulator separating the control gate from the floating gate, the metal oxide insulator having a second tunneling barrier height, the second tunneling barrier height being less than the first tunneling barrier height; a first metal layer separating the metal oxide insulator and the floating gate, the first metal layer in contact with the floating gate; a second metal layer separating the metal oxide insulator and the control gate, the metal layer in contact with the control gate, wherein the memory is adapted to operate the memory cell in a volatile memory mode and in a non-volatile memory mode. With regards to claim 13, and 27 Eldridge et al. disclose the control gate is a vertical control gate. With regards to claim 14 Eldridge et al. disclose the polysilicon edge defined control gate. With regards to 15 Eldridge et al. disclose a memory cell is controllable to access a first charge representing a data value from the storage capacitor in the volatile memory mode and a second charge representing a data value from the floating gate in the non-volatile memory mode such that the first charge is accessible without affecting the second charge and the second charge is accessible without affecting the first charge. With regards to claims 16-19 Eldridge et al. disclose a the particular metal oxide insulators. With regards to claim 20 Eldridge et al. disclose the floating gate includes a horizontally oriented floating gate in contact with the gate oxide. With regards to claims 21 and 25 Eldridge et al. disclose the gate oxide includes silicon oxide having a tunneling barrier height of about 3.2 eV (inherent), the floating gate includes polysilicon, and the control gate includes polysilicon. With regards to claim 23 Eldridge et al. disclose each memory cell is controllable to access a first charge

representing a data value from the storage capacitor in the volatile memory mode and a second charge representing a data value from the floating gate in the non-volatile memory mode such that the first charge is accessible without affecting the second charge and the second charge is accessible without affecting the first charge. With regards to claim 24 Eldridge et al. disclose wherein each memory cell further includes a first metal layer separating the floating gate and the metal oxide insulator, the first metal layer in contact with the metal oxide insulator, and a second metal layer separating the control gate and the metal oxide insulator, the second metal layer in contact with the metal oxide insulator.

The applied reference has a common inventor with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

4. Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by Yoshii et al. (US Patent 6,740,928). Yoshii et al. disclose a source region and a drain region separated by a channel region in a substrate; a storage capacitor coupled to one of the source and drain regions (the examiner is taking official notice that this is well known in the art) ; a floating gate opposing the channel region; a gate oxide separating the floating gate from the channel region, the gate oxide having a first tunneling barrier height; a control gate opposing the floating gate; and a metal oxide insulator separating

the control gate from the floating gate, the metal oxide insulator having a second tunneling barrier height, the second tunneling barrier height being less than the first tunneling barrier height, wherein the memory is adapted to operate the memory cell in a volatile memory mode and in a non-volatile memory mode (see figure 33).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Bradley K. Smith whose telephone number is (571) 272-1884. The examiner can normally be reached on 10-6 Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bill Baumeister can be reached on (571) 272-1722. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Brad Smith
Primary Examiner
Art Unit 2891